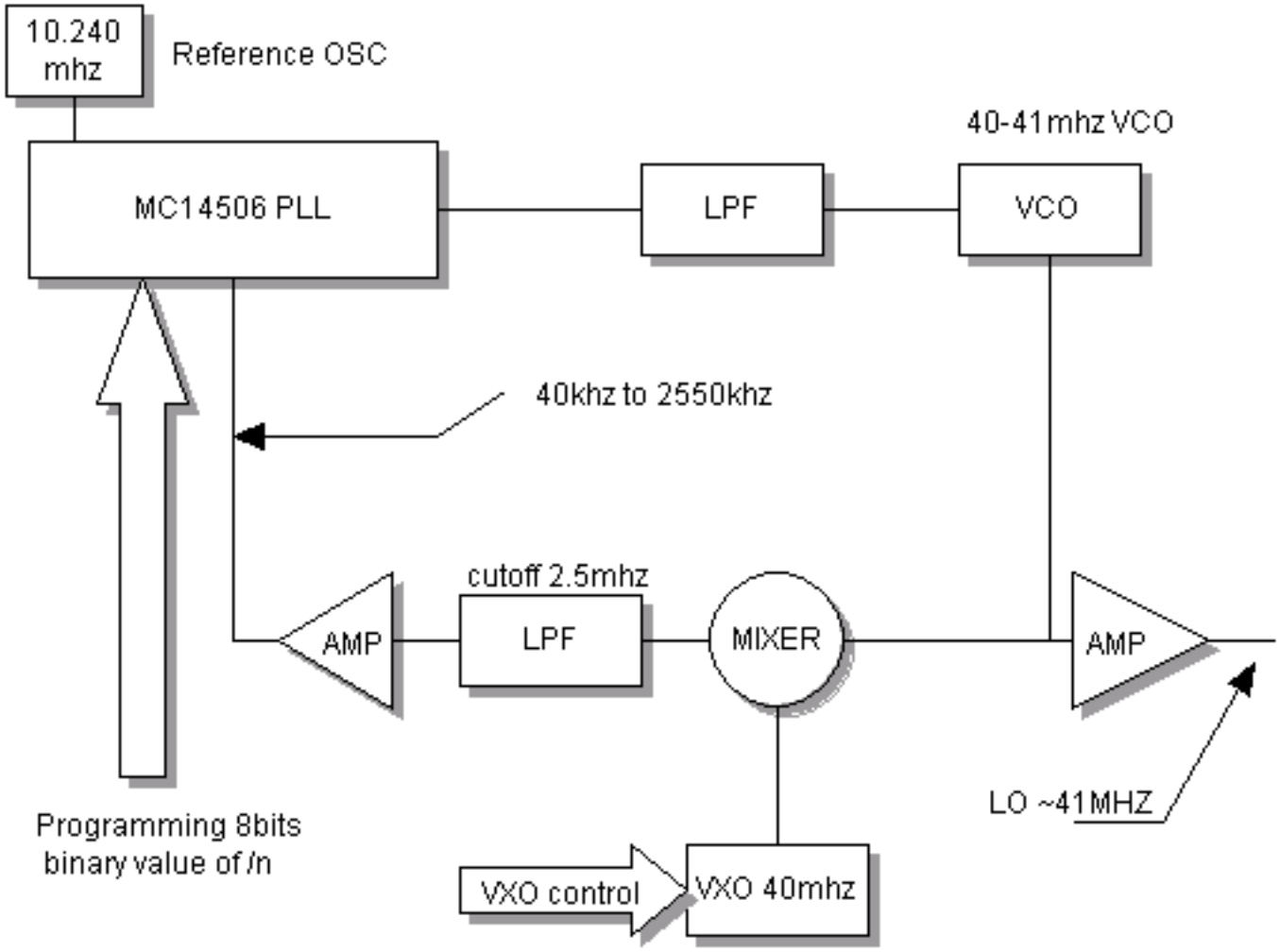

*Digitial steps are controlled by the PLL chip at 10KHZ
*By using a VXO it is easy to tune between the digital steps.
*Design is easily modified for new output frequencies.
*Uses simple PLL chip.

While fully digital tuning is desireable often it requires a very low reference frequency that can add considerable FM noise to the PLL output or a complex multi PLL system. By using a 10KHZ step the any incidental modulation of the control voltage is easily filtered. A benefit is that the range and total count used is low further reducing the phase noise of the PLL system. To interpolate between the 10khz digital steps a VXO is used to "tune" the output.

A secondary benefit is that the output of the PLL system is defined by the VXO frequency plus the reference (10KHZ) times the PLL /n modulus counter. Example the VXO is 40mhz and the /n counter is set to 10 the resuling frequency will be 100khz +40mhz =40.100mhz. The range of /n values can be from 4 to 255 or 40 to 2550khz. with a suitable VXO and VCO it's possible to tune a nearly 2.5mhz range. This makes the same design less sensitive to VCO and VXO changes.